段落の組み立て方

第5回

論文を構成する要素

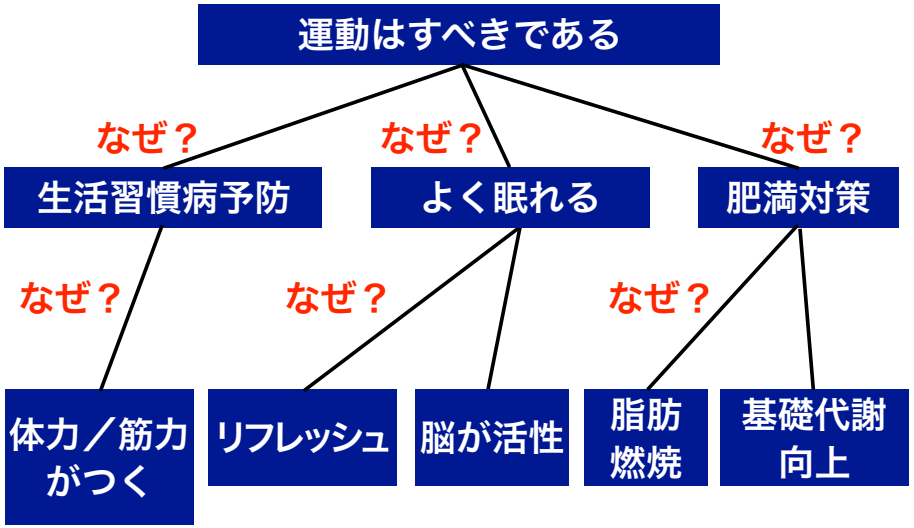
- 要約（abstract）
- 序論（introduction）
  - 論文の目的、問題の背景、議論の及ぶ範囲 **(Thesis)**

論文全体を通じて最も言いたいこと

- 本論（body）
  - 詳細な議論、それを裏付けるデータ
- 結論（conclusion）
  - 結果の総括、推論と判断
- 付録（appendix）
- 謝辞（acknowledgment）
- 参考文献（reference）

他の要素は「なぜ？」に答えるためにある

ピラミッド構造のおさらい



文章の構成単位

- 巻（volume）
- 号（number）
  - 部（part）
    - 章（chapter）
      - 節（section）
        - 段落（paragraph）
          - 文（sentence）

論文全体を通じて言いたいこと

各節で言いたいこと
各段落で言いたいこと
各文で言いたいこと

一般的な学術論文/レポート

必要に応じてサブセクションや
サブサブセクションを使う

段落（paragraph）とは？

- 文章における一つのまとまりのこと。通常は複数の文によって構成される。
- 行頭で1文字字下げを行うことから段落と呼ばれる。
- 段落では、一つの論点・小トピックについてのみ扱う。
  - したがって、段落が変わるとトピックが変わったことを意味する。
  - 一つの文だけからなる段落は原則書くべきでない。
  - 逆に長過ぎる段落も論点が明確でなくなるためよろしくない。バランスが大事。

論文を構成する３つの役割要素

- 3大構成要素
  - 序論（introduction）➔ 単独の節
    - 論文の目的、 問題の背景、議論の及ぶ範囲

      論文をまとめる上で一番難しい部分
  - 本論部分（body part）➔ 複数の節
    - 詳細な議論、それを裏付けるデータ
  - 結論（conclusion）➔ 単独の節
    - 結果の総括、推論と判断

節や段落内でも基本は同じ

良い文章の基本

- 良い文
  - 真の要点を簡潔にかつ正確に述べる。
    - 1 idea / 1 sentence でしたね？
- 良い文章の組み立ても基本は同じ（簡潔かつ正確）
  - 一つの段落では一つの論点（topic）を
    - 1 topic / 1 paragraph
  - 一つの節では一つの論題（subject）を
    - 1 subject / 1 section
  - 一つの論文では一つの主張（thesis）を
    - 1 thesis / 1 paper

段落（paragraph）の3つの要素

- トピック文（Topic Sentence）
  - 段落の論旨（段落内で最も主張したいこと）を表す文。段落の最初に書かれることもある。
- サポート文（Supporting Sentences）
  - トピック文をサポートするために、詳しく述べたり、具体的な例を挙げたり、統計を紹介する文。
- 結論＆リンク文（Concluding & Linking Sentence(s)）
  - 段落の結びや次の段落への橋渡しの文。 論旨を表すトピック文である場合もある。

段落の組み立て指針

A.　一つの段落には一つの概念や主張（トピック文）を盛ること。

B.　それぞれの段落には、なるべく初めの方に一般論に近い概念（導入文）や主張点（トピック文）を書いて読者の眼を引きつける。

C.　一つの概念には最低二つの例を示す（相反する例など）。

以降ルールA～Cとして表記

D. 段落のリンクを明確にする。

段落のリンクのさせ方

1. 前の段落の結論＆リンク文と段落の最初の文でキーワードを繰り返す。

2. キーとなる概念を繰り返す。

3. 似た文章を繰り返す。

4. 名詞を使って表現している文を代名詞に置き換える。

5. 前の段落と対比する内容で始める。

以降ルールD-1～D-5として表記

私の学生時代の論文を具体例として見てみましょう！

Fast-Acquisition PLL Synthesizer Using a Parallel N-Stage Cycle Swallower with Low Power Consumption and Low Phase Noise

Takahiko Saba, *Student Member, IEEE,* Duk-Kyu Park, *Member, IEEE,* and Shinsaku Mori, *Member, IEEE*

***Abstract*— A phase-locked loop (PLL) frequency synthesizer with an N-stage cycle swallower (NSCS) is one of the fastest frequency switching synthesizers, but the use of the NSCS results in high power consumption and phase noise in the UHF band. This paper elucidates these problems and proposes a fast-acquisition PLL synthesizer using a novel type of NSCS with low power consumption and low phase noise. Experimental results confirm that the use of a parallel NSCS and a prescalar results in greatly reduced power consumption and phase noise.**

I. Introduction

FREQUENCY hopping is a technique for using bandwidth efficiently by allowing several users to use the same band. There are two basic hopping patterns: *fast hopping,* which makes two or more hops for each symbol, and *slow hopping,* which makes two or more symbols for each hop. Although *slow hopping* does not serve the purpose of increasing capacity [1], *fast hopping* does because of its advantage of applying diversity. For *fast hopping,* frequency synthesizers with high-speed switching are essential. That is, a conventional PLL synthesizer generates an output frequency that is an integral multiple of the reference frequency. A low reference frequency governs the phase comparison frequency and thus the acquisition time of the PLL synthesizer. Moreover, the PLL synthesizer suffers from transients that limit the speed of acquisition [7]. Some methods for increasing the speed of acquisition have therefore been proposed [8]–[14].

One is the use of an N-stage cycle swallower (NSCS), which by removing pulses from the output signal pulse train of the synthesizer can allow the smallest frequency increment and the reference frequency to be independent of each other [11], [12]. A rapid acquisition time is obtained by using a higher reference frequency, and the acquisition time of a PLL synthesizer with the NSCS is more than two orders of magnitude faster than that of a conventional PLL synthesizer. The principle of the NSCS synthesizer is described in Section II.

An even better acquisition performance of the NSCS synthesizer has been attained by using multiple loop filters [13].

論文の中身

- 題材
  - 周波数ホッピング（来年前期のディジタル通信でやります）用の高速周波数切替シンセサイザ（周波数切替発振器）の低消費電力化と低位相雑音化に関して

序論（Introduction)の最初の部分を見ていきます

導入文（ルールB）：
「周波数ホッピングは、複数ユーザに同一の帯域を利用させることで、帯域を効率的に利用するための技術の一つである。」

I. INTRODUCTION

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B: 取り扱う話題の導入

296 IEEE TRANSACTIONS ON VEHICULAR TECHNOLOGY, VOL. 44, NO. 2, MAY 1995

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An even better acquisition performance of the NSCS synthesizer has been attained by using multiple loop filters [13].

サポート文：二つの例を挙げて説明（ルールC）
「ホッピングは基本的に高速ホッピングと低速ホッピングの二つに分類できる。（高速ホッピングの利点へ）」

I. INTRODUCTION

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C: 一つの概念に二つの例

結論＆リンク文：最も言いたいこと（ルールA）
「高速ホッピングのためには、高速スイッチングが可能な
周波数シンセサイザが不可欠である。」

I. Introduction

FREQUENCY hopping is a technique for using bandwidth efficiently by allowing several users to use the same band. There are two basic hopping patterns: *fast hopping*, which makes two or more hops for each symbol, and *slow hopping*, which makes t[illegible]or each hop. Although *slow hopping* d[illegible]e of increasing capacity [1], *fast hopping* does because of its advantage of applying diversity. For *fast hopping*, frequency synthesizers with high-speed switching are essential.

A: トピック文

diversity. For *fast hopping*, frequency synthesizers with high-speed switching are essential.

Frequency synthesizers are divided into two general types. The first includes all those that generate the desired output frequencie[illegible] from a source (or set of sources) by mixing, multiplying[illegible] including phase-locke[illegible]s is called *direct* and [illegible]ynthesizer (DDS), wh[illegible], [3]. The high power consumption of the DDS, however, makes it unsuitable for use in the portable radios in mobile communication systems.

C: 一つの概念には最低二つの例
D-1: キーワードを繰り返す

前の段落とのリンク文（ルールC、D-1）
「一般的に、周波数シンセサイザは二つに分類される。」

diversity. For *fast hopping*, frequency synthesizers with high-speed switching ar[illegible]

Frequency sy[illegible]sizers are divided into two general types.

C: 一つの概念には最低二つの例

The first includes all those that generate the desired output frequencies from a source (or set of sources) by mixing, multiplying, and dividing—or any other means not including phase-locked loops (PLL's). This class of synthesis is called *direct* and a typical example is the digital direct synthesizer (DDS), whose switching speed is extremely fast [2], [3]. The high power consumption of the DDS, however, makes it unsuitable for use in the portable radios in mobile communication systems.

サポート文：
二つの例の片方について、さらに利点／欠点の
相反する二つの例（ルールC）

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A: トピック文

結論文：トピック文（ルールA）
「DDSは、消費電力が大きいため、
移動通信システムの移動機には向かない。」

リンク文：二つの例の2番目を説明
（ルールC、D-5）

The first includes all those that generate the desired output frequencies from a source (or set of sources) by mixing, multiplying, and dividing, or any other means not including phase-locked lo called *direct* and a typ esizer (DDS), whose s . The high power consumption of the DDS, however, makes it unsuitable for use in the portable radios in mobile communication systems.

C: 一つの概念には最低二つの例
D-5: 前の段落と対比する内容

The second type of frequency synthesizer, called *indirect*, uses PLL's in its frequency-generating elements and is widely used in signal generators and radio communication equipment. Indeed, it is the implementation of the PLL in an integrated

The seco *indirect*, uses PLL's s widely used in signal generators and radio communication equipment.

C: 一つの概念には最低二つの例

Indeed, it is the implementation of the PLL in an integrated circuit that has led to inexpensive frequency synthesizers. In a conventional PLL synthesizer, the smallest frequency increment is the same as the reference frequency [4]–[6]. That is, a conventional PLL synthesizer generates an output frequency that is an integral multiple of the reference frequency. A low reference frequency governs the phase comparison frequency and thus the acquisition time of the PLL synthesizer. Moreover, the PLL synthesizer suffers from transients that limit the speed of acquisition [7]. Some methods

サポート文：二つ目の例について、
さらに利点／欠点の二つの例（ルールC）

トピック文（ルールA）
「基準周波数が低いと位相比較周波数も低くなり、
結果的にPLLシンセサイザの引き込み時間も遅くなる。」

circuit that has led to inexpensive frequency synthesizers. In a conventional PLL synthesizer, the smallest frequency increment is the same]–[6]. That is, a conventional PLL synthesizer generates an output frequency that is an integral multiple of the reference frequency. A low reference frequency governs the phase comparison frequency and thus the acquisition time of the PLL synthesizer. Moreover, the PLL synthesizer suffers from transients that limit the speed of acquisition [7]. Some methods for increasing the speed of acquisition have therefore been proposed [8]–[14].

A: トピック文

結論センテンス
「これらの理由から、引き込み速度を改善する手法が
いくつか提案されている。」

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次の段落へのリンクを意識

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A&B: トピック文
D-3: 似た文章を繰り返す
D-4: 名詞を代名詞に置き換え
D-5: 前の段落と対比する内容

トピック文（ルールA、B、D-3、4、5）

これから書く段落では何を言いたいのか？

日頃から意識しましょう

今読んでいる段落では何を言いたいのか？