Fast-Acquisition PLL Synthesizer Using a Parallel N-Stage Cycle Swallower with Low Power Consumption and Low Phase Noise

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***Abstract*— A phase-locked loop (PLL) frequency synthesizer with an N-stage cycle swallower (NSCS) is one of the fastest frequency switching synthesizers, but the use of the NSCS results in high power consumption and phase noise in the UHF band. This paper elucidates these problems and proposes a fast-acquisition PLL synthesizer using a novel type of NSCS with low power consumption and low phase noise. Experimental results confirm that the use of a parallel NSCS and a prescalar results in greatly reduced power consumption and phase noise.**

I. Introduction

FREQUENCY hopping is a technique for using bandwidth efficiently by allowing several users to use the same band. There are two basic hopping patterns: *fast hopping,* which makes two or more hops for each symbol, and *slow hopping,* which makes two or more symbols for each hop. Although *slow hopping* does not serve the purpose of increasing capacity [1], *fast hopping* does because of its advantage of applying diversity. For *fast hopping,* frequency synthesizers with high-speed switching are essential.

Frequency synthesizers are divided into two general types. The first includes all those that generate the desired output frequencies from a source (or set of sources) by mixing, multiplying, and dividing—or any other means not including phase-locked loops (PLL's). This class of synthesis is called *direct* and a typical example is the digital direct synthesizer (DDS), whose switching speed is extremely fast [2], [3]. The high power consumption of the DDS, however, makes it unsuitable for use in the portable radios in mobile communication systems.

The second type of frequency synthesizer, called *indirect,* uses PLL's in its frequency-generating elements and is widely used in signal generators and radio communication equipment. Indeed, it is the implementation of the PLL in an integrated circuit that has led to inexpensive frequency synthesizers. In a conventional PLL synthesizer, the smallest frequency increment is the same as the reference frequency [4]–[6]. That is, a conventional PLL synthesizer generates an output frequency that is an integral multiple of the reference frequency. A low reference frequency governs the phase comparison frequency and thus the acquisition time of the PLL synthesizer. Moreover, the PLL synthesizer suffers from transients that limit the speed of acquisition [7]. Some methods for increasing the speed of acquisition have therefore been proposed [8]–[14].

One is the use of an N-stage cycle swallower (NSCS), which by removing pulses from the output signal pulse train of the synthesizer can allow the smallest frequency increment and the reference frequency to be independent of each other [11], [12]. A rapid acquisition time is obtained by using a higher reference frequency, and the acquisition time of a PLL synthesizer with the NSCS is more than two orders of magnitude faster than that of a conventional PLL synthesizer. The principle of the NSCS synthesizer is described in Section II.

An even better acquisition performance of the NSCS synthesizer has been attained by using multiple loop filters [13]. During a frequency switching, the loop filters, which have various time constants, are switched. [14] describes a method for improving the output frequency accuracy of the NSCS synthesizer: precise output frequencies are obtained by varying the NSCS output frequency. This reference also shows that the acquisition time can be shortened by introducing an extra switching operation of division ratios in the NSCS. Despite these improvements, however, the NSCS synthesizer still has two problems in the UHF band: power consumption and phase noise.

This paper focuses on the reduction of power consumption as well as phase noise. To reduce power consumption, we use a simple prescalar. As detailed in Section III, however, this causes problems with phase noise because the NSCS may tend to remove two or more consecutive pulses of the synthesizer output signal.

To solve the phase noise problem, we propose a novel type of NSCS, one that has a parallel organization. Since the proposed parallel NSCS never removes pulses concentratively, phase noise is low. Furthermore, although to obtain a desirable output frequency accuracy when using only a prescalar we should use a 5-stage cycle swallower (5SCS), the proposed parallel NSCS can achieve the same output frequency accuracy with only a 3SCS. As a result, this method also leads to reduction in power consumption. This system is described in Section IV.

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In Section V, we present HF-band experimental results showing that our proposed NSCS consumes less than a quarter of the power required by the NSCS described in [11], [12] and that it suppresses more than 90% of the undesirable signals caused by phase noise. Our conclusions are presented in Section VI.

II. Synthesizers with an N-Stage Cycle Swallower

Fig. 1 shows a block diagram of the PLL synthesizer with the NSCS proposed in [11]–[14]. The synthesizer consists of a crystal oscillator, a phase detector, a low-pass filter, a voltage-controlled oscillator (VCO), the NSCS, and a programmable divider. With the NSCS removed, this synthesizer takes the familiar form of a conventional PLL synthesizer.

The structures of the NSCS and a cycle swallower are shown in Fig. 2; throughout the paper we call this type of NSCS the *serial* NSCS. As shown in Fig. 2(a), every cycle swallower, which is controlled by a coupled divider, is connected in series. The VCO output f_o is fed to both the first divider and the first cycle swallower (CS-1).

In the stage-i of the serial NSCS, one pulse of the CS-i input pulse train is removed whenever the carry output T_i, which serves as the trigger input of the CS-i, is generated by the divider-i. That is, the CS-i removes one pulse every M_i pulses,[1] where M_i $(1 \leq i \leq N)$ is the division ratio of the divider-i. The output frequency f_i of the CS-i is therefore given by

$$f_i = \left(1 - \frac{1}{M_i}\right) f_{i-1}. \tag{1}$$

With the generation of carry outputs T_i of the dividers from stage-1 to stage-N, cycle swallowers remove one pulse from each input pulse train. Therefore, using (1) we can write the output frequency f_N of the serial NSCS as

$$f_N = f_o \cdot \prod_{i=1}^{N} \left(1 - \frac{1}{M_i}\right). \tag{2}$$

The reference frequency f_r, which is equal to the feedback frequency f_b, is given by

$$f_r = f_b = \frac{f_N}{R} \tag{3}$$

where R is the ratio of the programmable divider shown in Fig. 1. Accordingly, the output frequency f_o of the synthesizer is

$$f_o = \frac{f_r \cdot R}{\prod_{i=1}^{N}\left(1 - \frac{1}{M_i}\right)}. \tag{4}$$

From these equations, we find that any output frequency is obtained by varying the set of division ratios (M_i, R).

A conventional PLL synthesizer generates an output frequency f_o that is an integral multiple of the reference frequency f_r. With the NSCS synthesizer, however, f_o can be independent of f_r because the NSCS removes pulses from the VCO output so that the feedback frequency f_b can be equal to f_r. Thus the smallest frequency increment Δf of the synthesizer is independent of the value of f_r; whereas the Δf of a conventional synthesizer is equal to f_r. Hence, a 100 times higher reference frequency leads to a 100 times shorter acquisition time.

[1] Note that pulses means periodic clock pulses with each pulse representing a frequency cycle, and removal of one pulse implies removal of one cycle of phase.

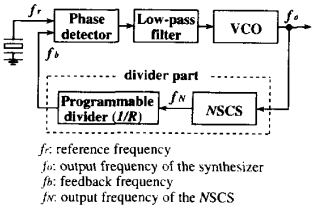


Fig. 1. Fast-switching PLL frequency synthesizer with an N-stage cycle swallower (NSCS).

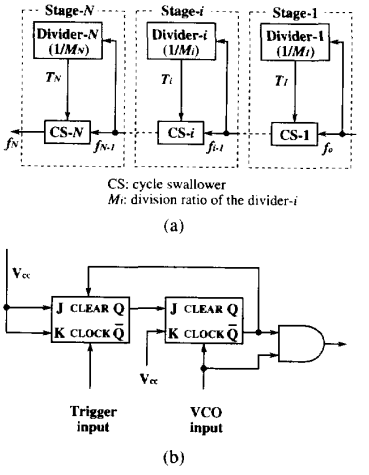


Fig. 2. N-stage cycle swallower (NSCS): (a) serial NSCS, (b) cycle swallower.

How are these division ratios to be selected? Because the programmable divider equalizes the pulse spacing of f_N, there are restrictions in determining the division ratios in the serial NSCS to avoid the concentrative pulse removal.

Fig. 3 illustrates some exaggerated examples of output waveforms in the serial 3SCS and the programmable divider. If every M_i is greater than R, the programmable divider may count equispaced (pulse-nonremoved) R pulses or inequispaced (pulse-removed) R pulses of the serial NSCS output; and if every M_i is too small, the serial NSCS may frequently remove two or more consecutive pulses from the VCO output. These cases cause unequal pulse spacing of f_b because the programmable divider cannot average the pulse spacing of f_N. Furthermore, this inequality causes phase noise that may appear in the VCO output spectrum as undesirable signals; these are peculiar features of the serial NSCS. These division ratios should therefore be smaller than the ratio of the programmable divider but should not be excessively small.

Table I, which presents some division ratios and corresponding output frequencies of the serial 3SCS synthesizer

TABLE I
SOME EXAMPLES OF DIVISION RATIOS IN THE SERIAL 3SCS SYNTHESIZER. Δf = 25 kHz, f_r =2.5 MHz, f_3: OUTPUT FREQUENCY OF THE 3SCS

CHANNEL ($\times 10^3$)	M_1	M_2	M_3	R	f_3 (Hz)	f_o (Hz)
1,425,000	340	341	342	565	1,412,500,000	1,425,000,000.0000
1,424,975	213	231	304	563	1,407,500,000	1,424,975,000.2031
1,424,950	82	277	281	559	1,397,500,000	1,424,950,000.1598
1,424,925	349	464	510	566	1,415,000,000	1,424,924,999.8939
1,418,900	295	378	495	563	1,407,500,000	1,418,899,999.9233
⋮	⋮	⋮	⋮	⋮	⋮	⋮
1,412,700	316	441	554	561	1,402,500,000	1,412,700,000.0000
1,412,675	341	466	467	561	1,402,500,000	1,412,675,000.0000
1,412,650	110	308	505	557	1,392,500,000	1,412,650,000.1660
1,412,625	325	454	525	561	1,402,500,000	1,412,624,999.8830
1,412,600	111	230	368	556	1,390,000,000	1,412,599,999.7837
⋮	⋮	⋮	⋮	⋮	⋮	⋮
1,400,100	51	358	359	546	1,365,000,000	1,400,100,000.0000
1,400,075	184	304	481	554	1,385,000,000	1,400,075,000.1503
1,400,050	100	447	469	552	1,380,000,000	1,400,050,000.1742
1,400,025	142	526	550	554	1,385,000,000	1,400,024,999.8308
1,400,000	418	419	420	556	1,390,000,000	1,400,000,000.0000

when f_r is 2.5 MHz and the Δf is 25 kHz, shows that even if f_r is higher than the Δf the serial NSCS synthesizer obtains each output frequency with a deviation within 0.415 Hz [14]. Certainly, every output frequency cannot have an accurate value; a large number of f_o deviate from their corresponding channel frequencies. As long as the deviation is small, however, this matters little because in practical mobile systems in the 1.5-GHz band portables are required to have a 2-ppm output frequency tolerance and base stations are required to have an output frequency tolerance of 0.5 ppm, which is about 750 Hz [15]. Of course, as more stages are used, output frequencies are obtained more accurately. But because the power consumption of the serial NSCS also increases with the increase of the number of stages, the number of stages should be as small as possible.

III. PROBLEMS WITH THE SERIAL NSCS SYNTHESIZER

A. Power Consumption

There has been an increasing need for UHF radio systems with low power dissipation, especially in portable radio systems. Since the lifetime of batteries for portable radios is determined by the current capacity of the batteries, the reduction of the current drain is essential in extending transceiver lifetime [16].

In a conventional PLL frequency synthesizer, when the output frequency band becomes high, the largest current drain is that of the programmable divider. The same is true for the serial NSCS because the input and the output of the serial NSCS have nearly the same frequency (see f_3 in Table I). That is, flip-flops (FF's) in the divider part of Fig. 1 (i.e., FF's in the serial NSCS and the programmable divider) operate at almost the same frequency.

Now, let us consider a UHF-band synthesizer (with a range from 1.4–1.425 GHz). We can see from Table I that every divider of the serial 3SCS and the programmable divider is required to be a 10-b binary counter (synchronous programmable divider). Assuming that the current drain of an FF is about 0.8 mA in this frequency range, we briefly estimate the total current drain of the divider part. As shown in Fig. 2(b), every cycle swallower has 2 FF's. Therefore there are 46 FF's in the divider part, and the total current is about 36.8 mA. This value is extremely high for portable use—and it is in practice difficult to implement a UHF-band programmable divider in an integrated circuit because all the various integrated circuits have a propagation delay, which may disturb the proper operation of division.

B. Phase Noise

When the frequency of the divider input is too high to permit proper operation of a programmable divider, prescalars can be used to lower that frequency. Since prescalars can often operate at higher frequencies because they do not have to allow for the delays involved in presetting [4], we must take into consideration the use of a prescalar to make a serial NSCS synthesizer operating in the UHF band.

Here we present some instances of division ratios and corresponding output frequencies in Table II when the prescalar is used with the following parameters.

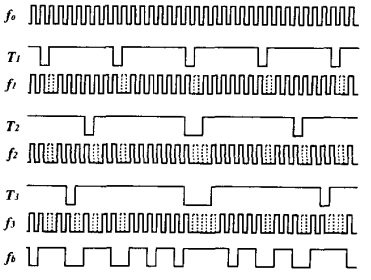
- Output frequency range: 1.4–1.425 GHz
- Reference frequency f_r: 2.5 MHz
- Smallest frequency increment Δf: 25 kHz
- Output frequency tolerance: ±0.2 ppm
- Type of NSCS: serial 5SCS
- Prescalar: divide-by-8.

The prescalar here is a 3-b ripple counter; that is, a divide-by-8 asynchronous counter. (Of course, the use of a dual modulus prescalar is more effective but here we use a single modulus one for convenience.) We also use a serial 5SCS to obtain output frequencies with deviation within ±0.2 ppm; this value is smaller than that in [15].

Under the assumption in Section III-A (0.8 mA per FF), this prescalar draws 1.4 mA of current and the range of the

TABLE II
SOME EXAMPLES OF DIVISION RATIOS IN THE SERIAL 5SCS SYNTHESIZER WITH A PRESCALAR. $\Delta f = 25$ kHz, $f_r = 2.5$ MHz, NSCS TYPE: SERIAL 5SCS, PRESCALAR: DIVIDE-BY-8

CHANNEL ($\times 10^3$)	M_1	M_2	M_3	M_4	M_5	R	f_o (Hz)
1,425,000	8	9	9	10	19	42	1,425,000,000.00
1,424,975	17	25	25	40	48	59	1,424,974,995.45
1,424,950	9	9	37	39	39	52	1,424,950,008.66
1,424,925	9	20	20	27	27	53	1,424,925,011.06
1,424,900	26	28	39	49	60	62	1,424,899,990.09
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1,412,700	10	20	25	37	40	55	1,412,699,999.44
1,412,675	13	15	38	48	57	57	1,412,675,006.75
1,412,650	12	47	51	56	60	60	1,412,650,024.06
1,412,625	30	33	44	45	50	62	1,412,624,993.86
1,412,600	16	20	46	48	48	59	1,412,600,001.59
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1,400,100	28	42	43	52	56	62	1,400,100,002.09
1,400,075	13	26	41	43	49	58	1,400,075,023.15
1,400,050	26	31	42	43	56	61	1,400,049,998.52
1,400,025	27	30	35	50	60	61	1,400,025,010.23
1,400,000	8	9	9	10	28	42	1,400,000,000.00

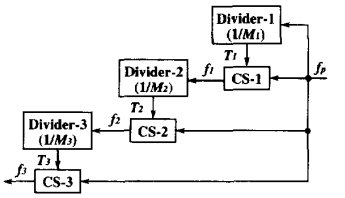


f_o: VCO output
f_b: programmable divider output
f_1, f_2, f_3: every output of the serial 3SCS
T_1, T_2, T_3: every output of the dividers
($M_1 = 8$, $M_2 = 10$, $M_3 = 11$, $R = 3$)

Fig. 3. Output waveforms of the serial 3SCS and the programmable divider.

prescalar output frequency (i.e., the range of the serial NSCS input frequency) is from 175 to 178.125 MHz. From Table II, we can see that every divider is a 6-b synchronous counter. There are therefore 46 FF's in the divider part. Here, assuming again that the current drain of an FF within the prescalar output range is about 0.2 mA, we obtain a current drain of about 9.2 mA. Consequently, the total current drain of the prescalar and the divider part is about 10.6 mA. This value is only one-third of the value described in Section III-A (36.8 mA). Thus we can obtain a lower current drain.

The use of the prescalar, however, causes a phase noise problem because it lowers the input and the output frequencies of the serial NSCS, and thus the value of R needed to keep f_b high. In Section II-B, we have already explained the restrictions in determining the division ratios in the serial NSCS, but as shown in Table II, in using the prescalar we have no choice but to preset small values for dividers. This violates the restrictions, leading to the concentrative pulse removal and thus becoming the major cause of phase noise.



f_p: output frequency of the prescalar

Fig. 4. Proposed parallel N-stage cycle swallower (parallel 3SCS).

IV. PROPOSED FREQUENCY SYNTHESIZER WITH A PARALLEL NSCS

A. Parallel NSCS

To solve the problems described in the previous section, we propose a novel PLL synthesizer that has a parallel NSCS and a prescalar. As shown in Fig. 4, every cycle swallower in the proposed parallel NSCS is connected in parallel and the prescalar output is fed to the divider-1 and all cycle swallowers.

To simplify the characteristics of the proposed parallel NSCS, we consider the parallel 3SCS. The output frequency of each cycle swallower is given as follows:

$$f_1 = \left(1 - \frac{1}{M_1}\right)\frac{1}{P} \cdot f_o \tag{5}$$

$$f_2 = \frac{1}{P} \cdot f_o - \frac{1}{M_2} \cdot f_1 \tag{6}$$

$$f_3 = \frac{1}{P} \cdot f_o - \frac{1}{M_3} \cdot f_2 \tag{7}$$

where P is the division ratio of the prescalar. Substituting (5) and (6) into (7), we can write

$$f_3 = \left(1 - \frac{1}{m_3}\right)\frac{1}{P} \cdot f_o \tag{8}$$

$$m_3 = \frac{M_1 M_2 M_3}{M_1 M_2 - M_1 + 1} \tag{9}$$

where m_3 is the nominal pulse removing interval of the last-stage cycle swallower. We can easily expand (8) and (9) to N stages in the same manner. The output frequency of the parallel NSCS is expressed as

$$f_N = \left(1 - \frac{1}{m_N}\right)\frac{1}{P} \cdot f_o \tag{10}$$

where

$$m_N = \frac{\prod_{i=1}^{N} M_i}{\sum_{k=1}^{N-1} \prod_{i=1}^{k} (-1)^{N-1+k} M_i + (-1)^{N-1}} \tag{11}$$

and the output frequency of the synthesizer is

$$f_o = \frac{f_r \cdot R \cdot P}{\left(1 - \frac{1}{m_N}\right)}. \tag{12}$$

TABLE III
SOME EXAMPLES OF DIVISION RATIOS OF THE PARALLEL 3SCS SYNTHESIZER WITH A PRESCALAR. Δf = 25 kHz, f_r = 2.5 MHz, NSCS TYPE: PARALLEL 3SCS, PRESCALAR: DIVIDE-BY-8

CHANNEL ($\times 10^3$)	M_1	M_2	M_3	R	f_o (Hz)
1,425.000	3	10	2	38	1,425,000,000.000
1,424,975	136	46	31	69	1,424,975,001.997
1,424,950	32	50	56	70	1,424,950,017.697
1,424,925	8	12	53	70	1,424,924,984.997
1,424,900	52	5	46	70	1,424,900,008.510
⋮	⋮	⋮	⋮	⋮	⋮
1,412,700	107	45	8	62	1,412,700,008.873
1,412,675	97	62	15	66	1,412,674,986.950
1,412,650	112	32	26	68	1,412,649,953.740
1,412,625	99	33	42	69	1,412,625,013.989
1,412,600	6	109	43	69	1,412,600,007.280
⋮	⋮	⋮	⋮	⋮	⋮
1,400,100	15	99	69	69	1,400,100,005.941
1,400,075	97	93	69	69	1,400,075,009.291
1,400,050	72	36	34	68	1,400,049,995.912
1,400,025	3	51	69	69	1,400,024,985.585
1,400,000	5	28	2	36	1,400,000,000.000

As shown in Fig. 4, since the pulse removal from the prescalar output f_p is conducted only by the last stage of the parallel 3SCS, the proposed parallel NSCS never removes two or more consecutive pulses. That is, it never removes pulses concentratively. The programmable divider can therefore easily average the pulse spacing of f_N, and thus phase noise mainly caused by unequal pulse spacing of f_b can be reduced.

Another advantage of the proposed parallel NSCS is that it can ease the restrictions in determining the ratio of the dividers described in Section II-B. Since the pulse removal from f_p is carried out only by the last stage of the parallel NSCS, the pulse removal in other stages hardly affects the pulse spacing of f_b. Therefore, the dividers in other stages can have division ratios higher than that of the programmable divider. The ratio of the last stage divider must be lower than that of the programmable divider. Practically, we might as well select the ratios of the dividers as follows: $M_i < R$ when $i = N$, and $M_i < 2R$ when $1 \le i \le N-1$.

Table III lists some examples of the division ratios of the proposed system with the following parameters.

- Output frequency range: 1.4–1.425 GHz
- Reference frequency f_r: 2.5 MHz
- Smallest frequency increment Δf: 25 kHz
- Output frequency tolerance: ±0.2 ppm
- Type of NSCS: parallel 3SCS
- Prescalar: divide-by-8.

The values listed in Table III show that the proposed parallel NSCS requires only three stages to obtain output frequency deviation within ±0.2 ppm, whereas as shown in Section III-B, the serial NSCS using a prescalar requires five stages. The proposed parallel NSCS is therefore also useful for reducing power consumption. In this case, the dividers are required to be 7-b synchronous counters, and the total current drain in the prescalar and the divider part is about 8.2 mA. This is less than three quarters of the value estimated in Section III-B for the serial NSCS synthesizer.

B. Loop Fundamentals

Consider the characteristics of the proposed loop when a lag-lead type loop filter and a phase/frequency detector (PFD) accompanied by a charge-pump are used in the feedback loop. In the loop, the charge-pump output has three states: an open-loop state for the phase-locked condition; and charging and discharging conditions of the loop filter when there is a large phase difference in the PFD. Therefore, the phase-locking process is identified by the behavior of the PLL using an active filter [17]. Here the transfer function $F(s)$ of the loop filter is given as

$$F(s) = \frac{s\tau_2 + 1}{s\tau_1} \tag{13}$$

where τ_1 and τ_2 are time constants of the loop filter.

The loop transfer function $H(s)$ is

$$H(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{14}$$

where

$$\omega_n = \left(\frac{K}{\tau_1}\right)^{1/2} \tag{15}$$

and

$$\zeta = \frac{\tau_2}{2}\left(\frac{K}{\tau_1}\right)^{1/2}. \tag{16}$$

Here ω_n is the natural frequency of the loop, ζ is the damping factor, and K is the loop gain, which is written as

$$K = \frac{K_v \cdot K_\phi}{P \cdot R}\left(1 - \frac{1}{m_N}\right) \tag{17}$$

where K_v is the VCO gain factor (rad/s/V) and K_ϕ is the PFD gain factor (V/rad).

Here the frequency response due to a frequency step ($\Delta\omega_{\text{out}} = 2\pi\Delta f_{\text{out}}$) is given as

$$\Phi(s) = [1 - H(s)]\frac{\Delta\omega_{out}}{s^2}. \tag{18}$$

Substituting (14) into (18) and taking derivatives of inverse Laplace transforms, we find the transient behavior to be

$$\Delta f_o(t) = \begin{cases} \Delta f_{out}\left(\cos\sqrt{1-\zeta^2}\,\omega_n t - \dfrac{\zeta}{\sqrt{1-\zeta^2}}\sin\sqrt{1-\zeta^2}\,\omega_n t\right)e^{-\zeta\omega_n t} & \text{for } \zeta < 1 \\ \Delta f_{out}(1-\omega_n t)e^{-\zeta\omega_n t} & \text{for } \zeta = 1. \\ \Delta f_{out}\left(\cosh\sqrt{\zeta^2-1}\,\omega_n t - \dfrac{\zeta}{\sqrt{\zeta^2-1}}\sinh\sqrt{\zeta^2-1}\,\omega_n t\right)e^{-\zeta\omega_n t} & \text{for } \zeta > 1 \end{cases} \tag{19}$$

By using (19) we can obtain a transient profile of the proposed parallel NSCS synthesizer.

TABLE IV
EXPERIMENTAL PARAMETERS

ITEMS	SPECIFICATIONS	
	NSCS synthesizer	Conventional synthesizer
f_o range	18.00–18.25 MHz	
f_o tolerance	±0.2 ppm	
Δf	250 Hz	
K_ϕ	$5/4\pi$ V/rad	
K_v	$2\pi\times$ 100 kHz/V	
Low-pass filter	Lag-lead filter	
ζ	1.0	
f_r	25 kHz	250 Hz
τ_1	27.0 ms	2.70 s
τ_2	17.7 ms	1.77 s
Type A	Serial 3SCS without a prescalar	—
Type B	Serial 5SCS with a divide-by-8 prescalar	—
Type C	Parallel 3SCS with a divide-by-8 prescalar	—

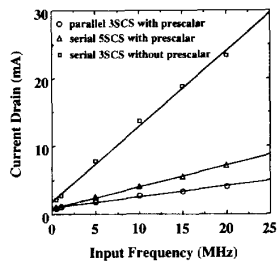


Fig. 5. Current drain characteristics of NSCS's (V_{cc} = 5 V).

V. EXPERIMENTAL RESULTS

To verify the characteristics of the proposed parallel NSCS synthesizer, we compared its performance with that of the serial one by using the experimental parameters listed in Table IV. In our HF-band experiment, we used commercial TTL, CMOS, and ECL devices for a PLL and we used programmable ASIC's (FPGA's) for prescalars, NSCS's, and programmable dividers. First in Section V-A, we report the measured current drain of the divider part of the three types of synthesizers listed in Table IV. Then to show the effect of phase noise on the VCO output, in Section V-B we report the measured VCO output spectra of the Type B and the Type C synthesizers. Finally in Section V-C, we report the results of comparing the acquisition performance of the proposed parallel NSCS synthesizer with that of the conventional PLL synthesizer.

A. Measurement of Current Drain

The measured current drain characteristics of the divider part of each of the three types of synthesizers are plotted in Fig. 5. This figure shows that at 18 MHz the current drain of the divider part in the proposed parallel NSCS synthesizer is less than a quarter that of the Type A synthesizer and about half that of the Type B synthesizer. The proposed parallel NSCS is therefore useful for reducing power consumption.

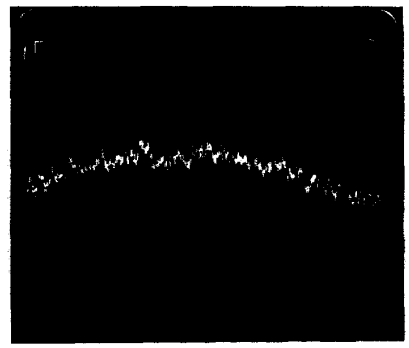


Fig. 6. Output spectrum of the serial 5SCS synthesizer with the prescalar (vertical: 10 dB/div., horizontal: 5 kHz/div., bandwidth: 300 Hz, center frequency: 18.0 MHz).

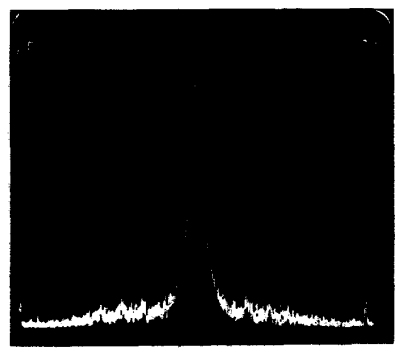


Fig. 7. Output spectrum of the parallel 3SCS synthesizer with the prescalar (vertical: 10 dB/div., horizontal: 5 kHz/div., bandwidth: 300 Hz, center frequency: 18.0 MHz).

B. Observation of VCO Output Spectrum

To examine the effect of phase noise on the VCO output signal, we observed the VCO output spectra of the Type B and the Type C synthesizers. For the serial 5SCS synthesizer with the divide-by-8 prescalar (Type B), when the values of M_1, M_2, M_3, M_4, M_5, and R are changed from 10, 14, 65, 71, 72, and 73 to 10, 11, 11, 12, 45, and 60, the VCO output frequency changes from 18.25 MHz to 18.00 MHz. The output spectrum at 18.00 MHz is shown in Fig. 6, which shows that a lot of undesirable signals appear in the VCO output signal.

For the proposed parallel 3SCS synthesizer with the divide-by-8 prescalar (Type C), when the values of M_1, M_2, M_3, and R are changed from 73, 40, 4, and 69 to 3, 30, 2, and 46, the VCO output frequency also changes from 18.25 MHz to 18.00 MHz. The output spectrum at 18.00 MHz is shown in Fig. 7. Comparing Fig. 6 with Fig. 7, we can see that the proposed synthesizer greatly reduces the phase noise: more than 90% of the undesirable signals present with the Type B synthesizer are suppressed.

C. Acquisition

To confirm the fast acquisition of the proposed parallel NSCS synthesizer, we compared its frequency acquisition process with that of the conventional synthesizer. The reference frequency of the proposed synthesizer was chosen to be 100 times higher than that of the conventional synthesizer, and

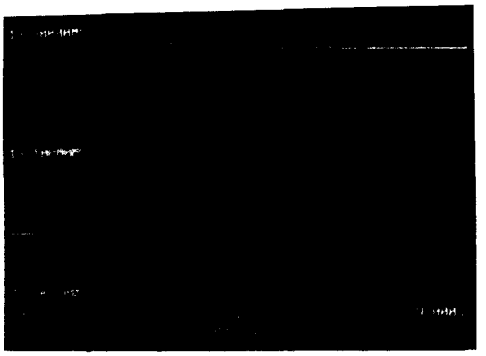


Fig. 8. Acquisition process of the conventional PLL synthesizer.

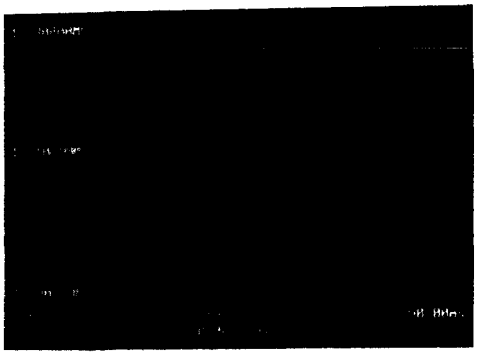


Fig. 9. Acquisition process of the parallel 3SCS synthesizer.

the time constants τ_1 and τ_2 were chosen so that the settling time[2] was 1000 cycles of each reference frequency when the damping factor $\zeta = 1$.

The frequency acquisition process of the two synthesizers, when the output frequencies were changed from 18.00 MHz to 18.25 MHz, are shown in Figs. 8 and 9, from which we can see that the frequency acquisition of the proposed synthesizer is 100 times faster than that of the conventional synthesizer.

VI. Conclusions

The proposed PLL synthesizer with the prescalar and the parallel NSCS produces much less phase noise than does a PLL synthesizer with a prescalar and a serial NSCS. Furthermore, when a prescalar is used, the parallel NSCS needs to have only three stages to attain the output accuracy produced by a serial NSCS with five stages. The proposed synthesizer thus reduces phase noise and power consumption. Experimental results in the HF band show that the parallel 3SCS synthesizer with a prescalar draws less than one quarter of the current drawn by the serial 3SCS synthesizer. Furthermore, the VCO output spectra can show that with the proposed synthesizer we suppress more than 90% of the undesirable signals present when using the serial 5SCS synthesizer with a prescalar.

[2] Settling time is usually defined as the time required for the phase error to be within the specified deviation (for example 5%) from the steady-state error [18], [19].

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References

[1] W. C. Y. Lee, "Overview of cellular CDMA," *IEEE Trans. Vehic. Technol.*, vol. 40, pp. 291–302, May 1991.
[2] J. Tierney, C. M. Radar, and B. Gold, "A digital frequency synthesizer," *IEEE Trans. Audio Electroacoust.*, vol. AU-19, pp. 48–57, Mar. 1971.
[3] V. Reinhardt, K. Gould, K. McNab, and M. Bustamante, "A short survey of frequency synthesizer techniques," in *Proc. IEEE 40th Annu. Frequency Control Symp.*, Sept. 1986, pp. 355–365.
[4] W. F. Egan, *Frequency Synthesis by Phase Lock.* New York: Wiley, 1981.
[5] U. L. Rohde, *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ: Prentice-Hall, 1983.
[6] V. Manassewitsch, *Frequency Synthesizers Theory and Design: Third Edition.* New York: Wiley, 1987.
[7] J. R. Alexovich and R. M. Gagliardi, "Effect of PLL frequency synthesizer in FSK frequency-hopped communications," *IEEE Trans. Commun.*, vol. 37, pp. 268–176, Mar. 1989.
[8] S. Saito, Y. Tarusawa, and H. Suzuki, "State-preserving intermittently locked loop (SPILL) frequency synthesizer for portable radio," *IEEE Trans. Microwave Theory Tech.*, vol. 37, pp. 1898–1903, Dec. 1989.
[9] A. Kajiwara and M. Nakagawa, "A new PLL frequency synthesizer with high switching speed," *IEEE Trans. Vehic. Technol.*, vol. 41, pp. 407–4013, Nov. 1992.
[10] K. Seki, M. Morimura, and S. Kato, "High resolution and fast frequency settling PLL synthesizer," *IEICE Trans. Commun.*, E75-B, no. 8, pp. 739–746, Aug. 1992.
[11] D. K. Park and S. Mori, "Fast acquisition frequency synthesizer with n-stage novel type cycle swallowers," in *Proc. IEEE ICC'92*, June 1992, pp. 496–500.
[12] ——, "Fast acquisition frequency synthesizer with multi-stage cycle swallowers," *Trans. IEICE*, vol. J75-B-II, pp. 515–523, Aug. 1992 (in Japanese).
[13] ——, "Fast acquisition frequency synthesizer with n-stage cycle swallowers, which switched the time constants of the loop filter," in *Proc. 1992 Joint Tech. Conf. Circuits/Syst. Computer and Commun.*, July 1992, pp. 168–173.
[14] T. Saba, D. K. Park, and S. Mori, "Fast acquisition PLL frequency synthesizer with improved N-stage cycle swallower," in *Proc. IEEE Pacific Rim Conf.'93*, May 1993, pp. 77–80.
[15] *The Ordinance for Regulating Radio Equipment of Japan.* 1993.
[16] S. Saito, T. Takada, and N. Kato, "A 5-mA 1-GHz GaAs dual-modulus prescalar IC," *IEEE J. Solid-State Circuits*, vol. 21, pp. 538–543, Aug. 1989.
[17] F. M. Gardner, "Charge-pump phase-lock loops," *IEEE Trans. Commun.*, vol. COM-28, pp. 1849-1858, Nov. 1980.
[18] H. M. Berlin, *The Phase-Locked Loop Bugbook, with Experiments.* E & L Instruments, Inc., 1978.
[19] J. Smith, *Modern Communication Circuits.* New York: McGraw-Hill, 1986.

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